WHAT IS CLAIMED IS:

1. An apparatus for use with an adder configured to generate a value and a leading one predictor configured to generate a leading one prediction corresponding to the value, the apparatus comprising a circuit coupled to receive the value and the leading one prediction, wherein the circuit is configured to generate an indication of whether or not the leading one prediction is correct responsive to the value and the leading one prediction.

2. The apparatus as recited in claim 1 further comprising a shifter coupled to receive the value and a shift amount indicated by the leading one prediction, wherein the shifter is configured to shift the value responsive to the shift amount to produce a shift result, and wherein the shifter shifts the value concurrent with the circuit generating the indication.

3. The apparatus as recited in claim 2 further comprising a second shifter coupled to receive the shift result and the indication, and wherein the second shifter is configured to shift the shift result one bit if the indication indicates that the leading one prediction is not correct.

4. The apparatus as recited in claim 1 wherein the leading one prediction is a one hot vector, and wherein each bit of the one hot vector corresponds to a different bit in the value.

5. The apparatus as recited in claim 4 wherein the circuit comprises a plurality of logic circuits, wherein each of the plurality of logic circuits is coupled to receive a bit of the value and a corresponding bit of the one hot vector and is configured to generate an output responsive to the bit and the corresponding bit.

6. The apparatus as recited in claim 5 further comprising a second logic circuit coupled

to receive the outputs of the plurality of logic circuits and configured to generate the indication responsive to the outputs.

7. The apparatus as recited in claim 6 wherein each of the plurality of logic circuits is an AND gate.

8. The apparatus as recited in claim 7 wherein the second logic circuit is configured to OR the outputs of the plurality of logic circuits.

9. The apparatus as recited in claim 1 wherein the value is a significand of a floating point number.

10. A floating point execution unit comprising:

an adder coupled to receive at least two significands and configured to generate an output significand in response thereto;

a leading one predictor coupled to receive the at least two significands and configured to generate a leading one prediction corresponding to the output significand in response to the at least two significands; and

a circuit coupled to receive the output significand and the leading one prediction, wherein the circuit is configured to generate an indication of whether or not the leading one prediction is correct responsive to the output significand and the leading one prediction.

11. The floating point execution unit as recited in claim 10 further comprising a shifter coupled to receive the output significand and a shift amount indicated by the leading one prediction, wherein the shifter is configured to shift the output significand responsive to

the shift amount to produce a shift result, and wherein the shifter shifts the output significand concurrent with the circuit generating the indication.

12. The floating point execution unit as recited in claim 11 further comprising a second shifter coupled to receive the shift result and the indication, and wherein the second shifter is configured to shift the shift result one bit if the indication indicates that the leading one prediction is not correct.

13. The floating point execution unit as recited in claim 10 wherein the leading one prediction is a one hot vector, and wherein each bit of the one hot vector corresponds to a different bit in the output significand.

14. The floating point execution unit as recited in claim 13 wherein the circuit comprises a plurality of logic circuits, wherein each of the plurality of logic circuits is coupled to receive a bit of the output significand and a corresponding bit of the one hot vector and is configured to generate an output responsive to the bit and the corresponding bit.

15. The floating point execution unit as recited in claim 14 further comprising a second logic circuit coupled to receive the outputs of the plurality of logic circuits and configured to generate the indication responsive to the outputs.

16. The floating point execution unit as recited in claim 15 wherein each of the plurality of logic circuits is an AND gate.

17. The floating point execution unit as recited in claim 16 wherein the second logic circuit is configured to OR the outputs of the plurality of logic circuits.

18. A method comprising:

receiving a value from an adder and a corresponding leading one prediction; and

determining if the leading one prediction is correct responsive to the value and the leading one prediction.

19. The method as recited in claim 18 further comprising shifting the value responsive to a shift amount indicated by the leading one prediction to produce a shift result, wherein the shifting is performed concurrent with the determining.

20. The method as recited in claim 19 further shifting the shift result one bit if the leading one prediction is not correct.

21. The method as recited in claim 18 wherein the leading one prediction is a one hot vector, and wherein each bit of the one hot vector corresponds to a different bit in the value.

22. The method as recited in claim 21 wherein the determining comprises logically combining each of the bits of the value with a corresponding bit of the one hot vector.

23. The method as recited in claim 22 wherein the determining further comprises logically combining a result of the logically combining each of the bits of the value with the corresponding bit of the one hot vector.

24. The method as recited in claim 23 wherein the logically combining each of the bits of the value with a corresponding bit of the one hot vector comprises logically ANDing the bits.

25. The method as recited in claim 24 wherein the logically combining the result comprises logically ORing the result.

26. The method as recited in claim 18 wherein the value is a significand of a floating point number.